

Applicant: Dan M. White  
Serial No.: 10/748,427  
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Attorney's Docket No.: Intel-017PUS  
Intel Docket Number: P17944

REMARKS

Claims 1 to 3, 5, 7, 9 to 13, 15 to 18, 20 and 24 to 32 are pending in this application of which claims 1, 13 and 16 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Applicants thank the Examiner and the Examiner's SPE for conducting an interview on August 15, 2007. Based on Applicants' arguments, the Examiner and the SPE agreed that a further prior art search would be conducted since the cited art does not teach Applicants' claims. Therefore, the Examiner and SPE agreed that the next action will not be made final.

Claims 1 to 3, 5, 7, 12, 13, 15 and 25 to 30 were rejected under 35 U.S.C. § 103(a) as being obvious over Bade et al. (U.S. Patent Publication Number 20020059054 hereinafter "Bade") in view of Mulchandani et al. (U.S. Patent Number 5,701,488 hereinafter "Mulchandani"). Claim 9 was rejected under 35 U.S.C. § 103(a) as being obvious over Bade in view of Mulchandani and Hoff et al. (U.S. Patent Number 5,778,231 hereinafter "Hoff"). Claim 10 was rejected under 35 U.S.C. § 103(a) as being obvious over Bade in view of Mulchandani and Hoff and in further view of Hall et al (U.S. Patent Number 4,720,778 hereinafter "Hall"). Claim 11 was rejected under 35 U.S.C. § 103(a) as being obvious over Bade in view of Mulchandani and in further view of Smith et al. (U.S. Patent Number 6,311,324 hereinafter "Smith"). Claims 16 to 18, 20, 31 and 32 were rejected under 35 U.S.C. § 103(a) as being obvious over Bade in view of Mulchandani, Hoff and in further view of Hall. Claim 24 was

rejected under 35 U.S.C. § 103(a) as being obvious over Bade in view of Mulchandani, Hoff, Hall and in further view of Smith.

Claim 1 is directed to a method of displaying embedded firmware program information. The method includes displaying a first screen to interact with a user for high level function selections, displaying a second screen to show hardware resources for a programmable circuit, displaying a third screen to show source code for a plurality of source code programs to control the programmable circuit and displaying a fourth screen to render symbolic information associated with the displayed source code. The symbolic information includes code labels, data labels referring to data structures including fields, data register names, and index register names; address locations for the code labels and the data labels; and listings associated with named registers, data labels for word, byte and short entities, and names of the data structures. The data structures and the fields of the data structures are individually expandable to show respective addresses and values of the word containing a start of the field.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, neither Bade nor Mulchandani whether taken separately or in combination discloses or suggests displaying a fourth screen to render symbolic information associated with the displayed source code where the symbolic information includes code labels, data labels referring to data structures comprising fields, data register names, and index register names, address locations for the code labels and the data labels, and listings including named registers, data labels for word, byte and short entities, and names of the data structures.

The Examiner has indicated that FIG. 36B of Bade, a debugger screen, teaches the fourth screen (see page 3 of the Office Action). However, FIG. 36B does not disclose or suggest that the symbolic information includes code labels, data labels referring to data structures comprising fields, data register names, and index register names, address locations for the code labels and the data labels, and listings including named registers, data labels for word, byte and short entities, and names of the data structures. Rather, the Examiner cites FIG. 26, a test bench tool bar, to show symbolic information, but refers to FIG. 31A, a library browser, which is a separate screen, to show data structures. Applicants submit that FIGS. 26, 31 and 36B unrelated to each other. Also, since FIGS. 26, 31 and 36B are two separate screens and a task bar that Bade does not teach, a single screen with the same symbolic information as recited in the claim 1.

Moreover, the symbolic information the Examiner cites in FIG. 36B is not the same as used in FIGS. 26 and 31, because FIGS. 26, 31 and 36B are used for different purposes. Applicants submit that the Examiner has improperly parsed the claim language so that the terms the Examiner is relying on in the cited art are being used inconsistently. The Examiner has therefore failed to show a single screen that has symbolic information with the same limitations as recited in claim 1. Thus, the FIGS. 26, 31 and 36B in Bade are not combinable to one of ordinary skill in the art.

Mulchandani does not teach a screen much less a screen as recited in claim 1. Accordingly, even if Mulchandani was combined with Bade, the hypothetical combination would not disclose or suggest a fourth screen to render symbolic information associated with the displayed source code where the symbolic information includes code labels, data labels referring

to data structures comprising fields, data register names, and index register names, address locations for the code labels and the data labels, and listings including named registers, data labels for word, byte and short entities, and names of the data structures as recited in claim 1.

Applicants respectfully submit that the combination of the Bade and Mulchandani references would not be made by one of ordinary skill in the art. For example, Mulchandani includes information on a Bus State Analyzer whereas FIG. 26 is a tool bench task bar, FIG. 31 of Bade includes data on libraries and FIG. 36B includes data for debugging, none of which includes a bus state analyzer. Thus, the combination of the cited references in the manner suggested by the Examiner is a hindsight reconstruction made possible only by using Applicants' specification.

In addition, one of ordinary skill in the art would not have reasonably expected success by making the Examiner's suggested combination since combining a bus state analyzer with a library, a task bar and a debugger could not perform the recited limitations in claim 1.

Furthermore, the cited art, whether taken separately or in combination, does not disclose or suggest that the data structures and the fields of the data structures are individually expandable to show respective addresses and values of the word containing a start of the field.

The Examiner has indicated that Bade teaches data structures that are expandable. However, Bade does not teach values of the word containing a start of the field nor has the Examiner specifically shown where this limitation may be found in the cited art. Mulchandani does not disclose or suggest that the fields of the data structures are individually expandable

much less teach that the fields of the data structures are individually expandable to show respective addresses and values of the word containing a start of the field nor has the Examiner made such an assertion in the office Action. Since neither reference teaches values of the word containing a start of the field, the suggest combination would not teach the recited limitation either. Therefore, Applicants respectfully submit that the Examiner has not established a *prima facie* rejection.

Claims 13 and 16 include the corresponding feature that the data structures and the fields of the data structures are individually expandable to show respective addresses and values of the word containing a start of the field as recited in claim 1. Applicant submits that the cited art should also be withdrawn with respect to claims 13 and 18 for at least the same reasons as claim 1.

Applicant submits that all dependent claims now depend on allowable independent claims.

For at least the foregoing reasons, Applicant requests withdrawal of the art rejections.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for withdrawing the prior art cited with regards to any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as

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specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

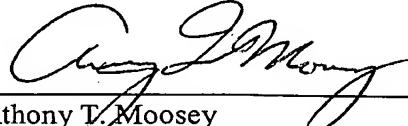
Applicant submits that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

Applicant's attorney can be reached by telephone at (781) 401-9988 ext. 123.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: Intel-017PUS.

Respectfully submitted,

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